Laboratory Report

**Course:** Coen 316 **Lab Section:** DL-X

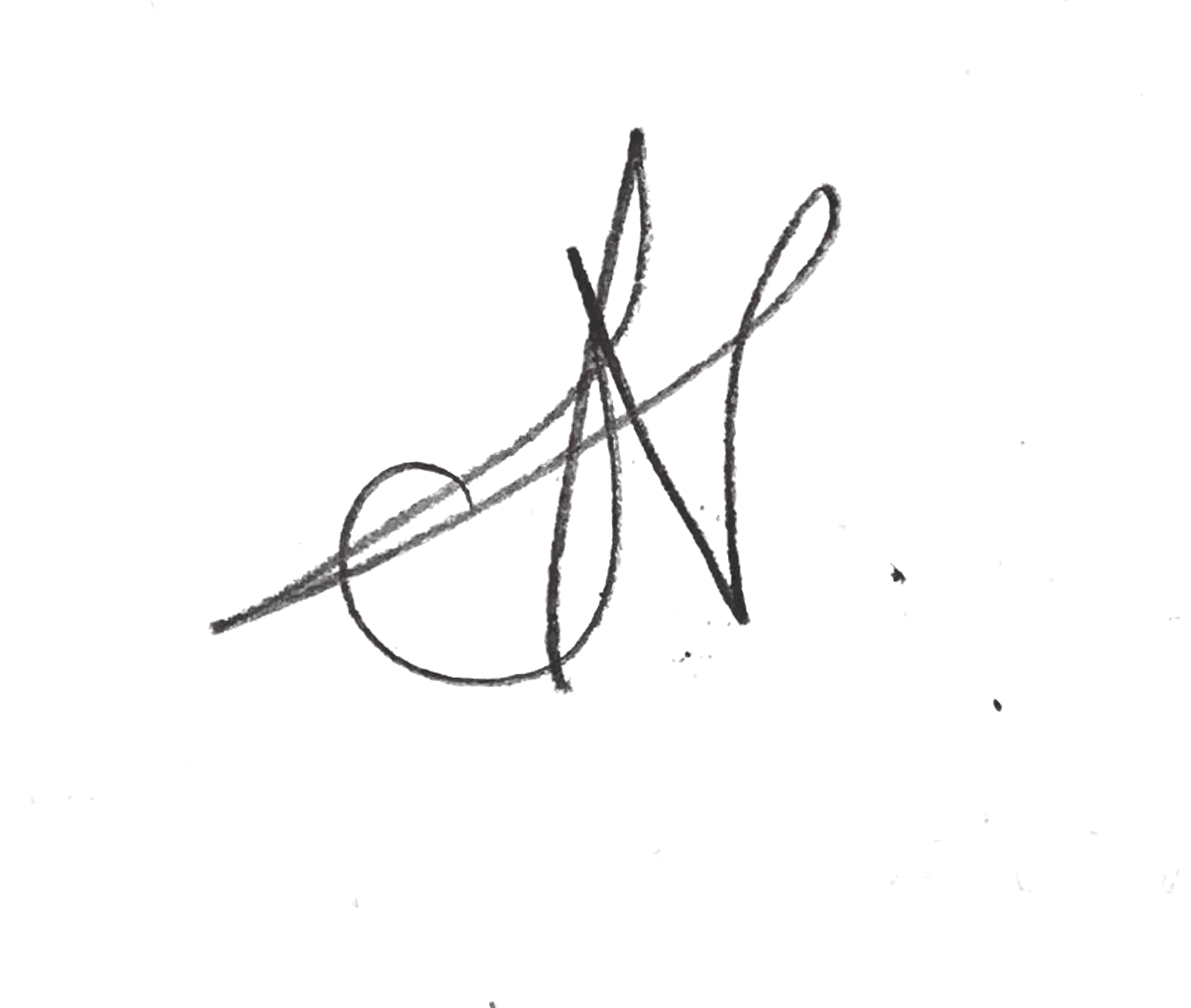
**Experiment No:** 3 **Date Performed:** 2023 – 10 – 26

**Report Due Date:** 2023 – 11 – 09

**Name:** Noah Louvet **ID:** 40086114

**I certify that this submission is my original work and meets the Faculty’s Expectations of Originality**

**Signature:**  **Date:** 2023 – 10 – 05



**Objectives**

In this lab, the main objectives are to comprehen the encoding format of jump and branch instructions in a processor. The focus is on implementing the Next-Address unit, which is responsible for generating the next address for the Program Counter (PC) register. The lab aims to differentiate between various instruction types such as unconditional jumps, conditional branches, and jump register instructions. Additionally, the objectives include analyzing the inputs, control signals, and logic involved in calculating the next address for different types of instructions.

**Introduction**

The Next-Address unit is crucial in determining the next instruction to be executed. By considering different instruction types, such as unconditional jumps, conditional branches, and jump register instructions, this unit calculates the appropriate next address. Key inputs, including the PC value, register contents, and specific control signals, are utilized to make these calculations.

The following entity is provided in the lab manual as a starting block for our vhdl code:

A white text with black text

Description automatically generated

***Figure 1***: Entity specification (source : lab manual)

A diagram of a machine

Description automatically generated

***Figure 2***: diagram

**Results**

In this part I’ll be showing the results of the conducted lab with screenshots at every step as well as the different codes used to obtain the results.

**32-bit source code:**

A screen shot of a computer code

Description automatically generated

A screenshot of a computer code

Description automatically generated

***Figure 3*:** nextaddress.vhd

**A screenshot of a computer program

Description automatically generated**

**A screenshot of a computer program

Description automatically generated**

***Figure 4*:** Board wrapper (4-bit version)

**A screenshot of a computer code

Description automatically generated**

***Figure 5*:** Contraints file .xdc

**A screenshot of a document

Description automatically generated**

***Figure 6*:** modelsim waveform

A screenshot of a computer

Description automatically generated



**A screenshot of a computer program

Description automatically generated**

**A screenshot of a computer code

Description automatically generated**

**A screenshot of a computer code

Description automatically generated**

***Figure 7*:** DO file

Vivado logs can be found in the appendix section.

**Appendix**

The logs contained some warnings due to the unused bits as the board can only accommodate for 4 bits, the synthesis and implementation as well as generation of the bistream were successful as these warnings can be neglected.

**Vivado Synthesis**

\*\*\* Running vivado

with args -log next\_address.vdi -applog -m64 -product Vivado -messageDb vivado.pb -mode batch -source next\_address.tcl -notrace

\*\*\*\*\*\* Vivado v2018.2 (64-bit)

\*\*\*\* SW Build 2258646 on Thu Jun 14 20:02:38 MDT 2018

\*\*\*\* IP Build 2256618 on Thu Jun 14 22:10:49 MDT 2018

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source next\_address.tcl -notrace

Command: link\_design -top next\_address -part xc7a100tcsg324-1

Design is defaulting to srcset: sources\_1

Design is defaulting to constrset: constrs\_1

INFO: [Netlist 29-17] Analyzing 14 Unisim elements for replacement

INFO: [Netlist 29-28] Unisim Transformation completed in 0 CPU seconds

INFO: [Project 1-479] Netlist was created with Vivado 2018.2

INFO: [Device 21-403] Loading part xc7a100tcsg324-1

INFO: [Project 1-570] Preparing netlist for logic optimization

Parsing XDC File [/nfs/home/n/n\_louvet/Coen316/lab3/vivado/lab3\_316/lab3\_316.srcs/constrs\_1/imports/DO/next\_address.xdc]

Finished Parsing XDC File [/nfs/home/n/n\_louvet/Coen316/lab3/vivado/lab3\_316/lab3\_316.srcs/constrs\_1/imports/DO/next\_address.xdc]

INFO: [Opt 31-138] Pushed 0 inverter(s) to 0 load pin(s).

INFO: [Project 1-111] Unisim Transformation Summary:

No Unisim elements were transformed.

7 Infos, 0 Warnings, 0 Critical Warnings and 0 Errors encountered.

link\_design completed successfully

link\_design: Time (s): cpu = 00:00:07 ; elapsed = 00:00:30 . Memory (MB): peak = 1652.379 ; gain = 344.242 ; free physical = 10470 ; free virtual = 22613

Command: opt\_design

Attempting to get a license for feature 'Implementation' and/or device 'xc7a100t'

INFO: [Common 17-349] Got license for feature 'Implementation' and/or device 'xc7a100t'

Running DRC as a precondition to command opt\_design

Starting DRC Task

INFO: [DRC 23-27] Running DRC with 8 threads

INFO: [Project 1-461] DRC finished with 0 Errors

INFO: [Project 1-462] Please refer to the DRC report (report\_drc) for more information.

Time (s): cpu = 00:00:01 ; elapsed = 00:00:03 . Memory (MB): peak = 1745.406 ; gain = 93.027 ; free physical = 10461 ; free virtual = 22604

Starting Cache Timing Information Task

INFO: [Timing 38-35] Done setting XDC timing constraints.

Ending Cache Timing Information Task | Checksum: 247d03c66

Time (s): cpu = 00:00:09 ; elapsed = 00:00:38 . Memory (MB): peak = 2166.902 ; gain = 421.496 ; free physical = 10002 ; free virtual = 22166

Starting Logic Optimization Task

Phase 1 Retarget

INFO: [Opt 31-138] Pushed 0 inverter(s) to 0 load pin(s).

INFO: [Opt 31-49] Retargeted 0 cell(s).

Phase 1 Retarget | Checksum: 247d03c66

Time (s): cpu = 00:00:00 ; elapsed = 00:00:00.01 . Memory (MB): peak = 2166.902 ; gain = 0.000 ; free physical = 10050 ; free virtual = 22213

INFO: [Opt 31-389] Phase Retarget created 0 cells and removed 0 cells

Phase 2 Constant propagation

INFO: [Opt 31-138] Pushed 0 inverter(s) to 0 load pin(s).

Phase 2 Constant propagation | Checksum: 247d03c66

Time (s): cpu = 00:00:00 ; elapsed = 00:00:00.01 . Memory (MB): peak = 2166.902 ; gain = 0.000 ; free physical = 10050 ; free virtual = 22213

INFO: [Opt 31-389] Phase Constant propagation created 0 cells and removed 0 cells

Phase 3 Sweep

Phase 3 Sweep | Checksum: 247d03c66

Time (s): cpu = 00:00:00 ; elapsed = 00:00:00.01 . Memory (MB): peak = 2166.902 ; gain = 0.000 ; free physical = 10050 ; free virtual = 22213

INFO: [Opt 31-389] Phase Sweep created 0 cells and removed 0 cells

Phase 4 BUFG optimization

Phase 4 BUFG optimization | Checksum: 247d03c66

Time (s): cpu = 00:00:00 ; elapsed = 00:00:00.01 . Memory (MB): peak = 2166.902 ; gain = 0.000 ; free physical = 10050 ; free virtual = 22213

INFO: [Opt 31-662] Phase BUFG optimization created 0 cells of which 0 are BUFGs and removed 0 cells.

Phase 5 Shift Register Optimization

Phase 5 Shift Register Optimization | Checksum: 247d03c66

Time (s): cpu = 00:00:00.01 ; elapsed = 00:00:00.01 . Memory (MB): peak = 2166.902 ; gain = 0.000 ; free physical = 10050 ; free virtual = 22213

INFO: [Opt 31-389] Phase Shift Register Optimization created 0 cells and removed 0 cells

Phase 6 Post Processing Netlist

Phase 6 Post Processing Netlist | Checksum: 247d03c66

Time (s): cpu = 00:00:00.01 ; elapsed = 00:00:00.01 . Memory (MB): peak = 2166.902 ; gain = 0.000 ; free physical = 10050 ; free virtual = 22213

INFO: [Opt 31-389] Phase Post Processing Netlist created 0 cells and removed 0 cells

Starting Connectivity Check Task

Time (s): cpu = 00:00:00 ; elapsed = 00:00:00 . Memory (MB): peak = 2166.902 ; gain = 0.000 ; free physical = 10050 ; free virtual = 22213

Ending Logic Optimization Task | Checksum: 247d03c66

Time (s): cpu = 00:00:00.01 ; elapsed = 00:00:00.02 . Memory (MB): peak = 2166.902 ; gain = 0.000 ; free physical = 10050 ; free virtual = 22213

Starting Power Optimization Task

INFO: [Pwropt 34-132] Skipping clock gating for clocks with a period < 2.00 ns.

Ending Power Optimization Task | Checksum: 247d03c66

Time (s): cpu = 00:00:00.01 ; elapsed = 00:00:00.03 . Memory (MB): peak = 2166.906 ; gain = 0.004 ; free physical = 10050 ; free virtual = 22213

Starting Final Cleanup Task

Ending Final Cleanup Task | Checksum: 247d03c66

Time (s): cpu = 00:00:00 ; elapsed = 00:00:00 . Memory (MB): peak = 2166.906 ; gain = 0.000 ; free physical = 10050 ; free virtual = 22213

INFO: [Common 17-83] Releasing license: Implementation

23 Infos, 0 Warnings, 0 Critical Warnings and 0 Errors encountered.

opt\_design completed successfully

opt\_design: Time (s): cpu = 00:00:10 ; elapsed = 00:00:41 . Memory (MB): peak = 2166.906 ; gain = 514.527 ; free physical = 10050 ; free virtual = 22213

INFO: [Timing 38-480] Writing timing data to binary archive.

Writing placer database...

Writing XDEF routing.

Writing XDEF routing logical nets.

Writing XDEF routing special nets.

Write XDEF Complete: Time (s): cpu = 00:00:00.07 ; elapsed = 00:00:00.11 . Memory (MB): peak = 2198.922 ; gain = 0.004 ; free physical = 10048 ; free virtual = 22212

INFO: [Common 17-1381] The checkpoint '/nfs/home/n/n\_louvet/Coen316/lab3/vivado/lab3\_316/lab3\_316.runs/impl\_1/next\_address\_opt.dcp' has been generated.

INFO: [runtcl-4] Executing : report\_drc -file next\_address\_drc\_opted.rpt -pb next\_address\_drc\_opted.pb -rpx next\_address\_drc\_opted.rpx

Command: report\_drc -file next\_address\_drc\_opted.rpt -pb next\_address\_drc\_opted.pb -rpx next\_address\_drc\_opted.rpx

INFO: [IP\_Flow 19-234] Refreshing IP repositories

INFO: [IP\_Flow 19-1704] No user IP repositories specified

INFO: [IP\_Flow 19-2313] Loaded Vivado IP repository '/CMC/tools/xilinx/Vivado\_2018.2/Vivado/2018.2/data/ip'.

INFO: [DRC 23-27] Running DRC with 8 threads

INFO: [Coretcl 2-168] The results of DRC are in file /nfs/home/n/n\_louvet/Coen316/lab3/vivado/lab3\_316/lab3\_316.runs/impl\_1/next\_address\_drc\_opted.rpt.

report\_drc completed successfully

report\_drc: Time (s): cpu = 00:00:03 ; elapsed = 00:00:05 . Memory (MB): peak = 2278.961 ; gain = 80.031 ; free physical = 10009 ; free virtual = 22173

Command: place\_design

Attempting to get a license for feature 'Implementation' and/or device 'xc7a100t'

INFO: [Common 17-349] Got license for feature 'Implementation' and/or device 'xc7a100t'

INFO: [DRC 23-27] Running DRC with 8 threads

INFO: [Vivado\_Tcl 4-198] DRC finished with 0 Errors

INFO: [Vivado\_Tcl 4-199] Please refer to the DRC report (report\_drc) for more information.

Running DRC as a precondition to command place\_design

INFO: [DRC 23-27] Running DRC with 8 threads

INFO: [Vivado\_Tcl 4-198] DRC finished with 0 Errors

INFO: [Vivado\_Tcl 4-199] Please refer to the DRC report (report\_drc) for more information.

Starting Placer Task

INFO: [Place 30-611] Multithreading enabled for place\_design using a maximum of 8 CPUs

Phase 1 Placer Initialization

Phase 1.1 Placer Initialization Netlist Sorting

Netlist sorting complete. Time (s): cpu = 00:00:00 ; elapsed = 00:00:00 . Memory (MB): peak = 2278.961 ; gain = 0.000 ; free physical = 10005 ; free virtual = 22169

Phase 1.1 Placer Initialization Netlist Sorting | Checksum: 1922bfd7b

Time (s): cpu = 00:00:00 ; elapsed = 00:00:00.01 . Memory (MB): peak = 2278.961 ; gain = 0.000 ; free physical = 10005 ; free virtual = 22169

Netlist sorting complete. Time (s): cpu = 00:00:00 ; elapsed = 00:00:00 . Memory (MB): peak = 2278.961 ; gain = 0.000 ; free physical = 10005 ; free virtual = 22169

Phase 1.2 IO Placement/ Clock Placement/ Build Placer Device

INFO: [Timing 38-35] Done setting XDC timing constraints.

Phase 1.2 IO Placement/ Clock Placement/ Build Placer Device | Checksum: 1922bfd7b

Time (s): cpu = 00:00:00.58 ; elapsed = 00:00:00.37 . Memory (MB): peak = 2278.961 ; gain = 0.000 ; free physical = 9997 ; free virtual = 22161

Phase 1.3 Build Placer Netlist Model

Phase 1.3 Build Placer Netlist Model | Checksum: 213b84558

Time (s): cpu = 00:00:00.63 ; elapsed = 00:00:00.39 . Memory (MB): peak = 2278.961 ; gain = 0.000 ; free physical = 9998 ; free virtual = 22161

Phase 1.4 Constrain Clocks/Macros

Phase 1.4 Constrain Clocks/Macros | Checksum: 213b84558

Time (s): cpu = 00:00:00.64 ; elapsed = 00:00:00.39 . Memory (MB): peak = 2278.961 ; gain = 0.000 ; free physical = 9998 ; free virtual = 22161

Phase 1 Placer Initialization | Checksum: 213b84558

Time (s): cpu = 00:00:00.64 ; elapsed = 00:00:00.39 . Memory (MB): peak = 2278.961 ; gain = 0.000 ; free physical = 9998 ; free virtual = 22161

Phase 2 Global Placement

Phase 2.1 Floorplanning

Phase 2.1 Floorplanning | Checksum: 213b84558

Time (s): cpu = 00:00:00.67 ; elapsed = 00:00:00.41 . Memory (MB): peak = 2278.961 ; gain = 0.000 ; free physical = 9996 ; free virtual = 22160

WARNING: [Place 46-29] place\_design is not in timing mode. Skip physical synthesis in placer

Phase 2 Global Placement | Checksum: 24ab3894c

Time (s): cpu = 00:00:01 ; elapsed = 00:00:00.55 . Memory (MB): peak = 2352.984 ; gain = 74.023 ; free physical = 9975 ; free virtual = 22139

Phase 3 Detail Placement

Phase 3.1 Commit Multi Column Macros

Phase 3.1 Commit Multi Column Macros | Checksum: 24ab3894c

Time (s): cpu = 00:00:01 ; elapsed = 00:00:00.56 . Memory (MB): peak = 2352.984 ; gain = 74.023 ; free physical = 9975 ; free virtual = 22139

Phase 3.2 Commit Most Macros & LUTRAMs

Phase 3.2 Commit Most Macros & LUTRAMs | Checksum: 2370ee589

Time (s): cpu = 00:00:02 ; elapsed = 00:00:00.58 . Memory (MB): peak = 2352.984 ; gain = 74.023 ; free physical = 9975 ; free virtual = 22138

Phase 3.3 Area Swap Optimization

Phase 3.3 Area Swap Optimization | Checksum: 1b9ab68f2

Time (s): cpu = 00:00:02 ; elapsed = 00:00:00.58 . Memory (MB): peak = 2352.984 ; gain = 74.023 ; free physical = 9975 ; free virtual = 22138

Phase 3.4 Pipeline Register Optimization

Phase 3.4 Pipeline Register Optimization | Checksum: 1b9ab68f2

Time (s): cpu = 00:00:02 ; elapsed = 00:00:00.58 . Memory (MB): peak = 2352.984 ; gain = 74.023 ; free physical = 9975 ; free virtual = 22138

Phase 3.5 Small Shape Detail Placement

Phase 3.5 Small Shape Detail Placement | Checksum: 1d1cffe7a

Time (s): cpu = 00:00:02 ; elapsed = 00:00:00.68 . Memory (MB): peak = 2352.984 ; gain = 74.023 ; free physical = 9971 ; free virtual = 22135

Phase 3.6 Re-assign LUT pins

Phase 3.6 Re-assign LUT pins | Checksum: 1d1cffe7a

Time (s): cpu = 00:00:02 ; elapsed = 00:00:00.68 . Memory (MB): peak = 2352.984 ; gain = 74.023 ; free physical = 9971 ; free virtual = 22135

Phase 3.7 Pipeline Register Optimization

Phase 3.7 Pipeline Register Optimization | Checksum: 1d1cffe7a

Time (s): cpu = 00:00:02 ; elapsed = 00:00:00.68 . Memory (MB): peak = 2352.984 ; gain = 74.023 ; free physical = 9971 ; free virtual = 22135

Phase 3 Detail Placement | Checksum: 1d1cffe7a

Time (s): cpu = 00:00:02 ; elapsed = 00:00:00.68 . Memory (MB): peak = 2352.984 ; gain = 74.023 ; free physical = 9971 ; free virtual = 22135

Phase 4 Post Placement Optimization and Clean-Up

Phase 4.1 Post Commit Optimization

Phase 4.1 Post Commit Optimization | Checksum: 1d1cffe7a

Time (s): cpu = 00:00:02 ; elapsed = 00:00:00.68 . Memory (MB): peak = 2352.984 ; gain = 74.023 ; free physical = 9971 ; free virtual = 22135

Phase 4.2 Post Placement Cleanup

Phase 4.2 Post Placement Cleanup | Checksum: 1d1cffe7a

Time (s): cpu = 00:00:02 ; elapsed = 00:00:00.69 . Memory (MB): peak = 2352.984 ; gain = 74.023 ; free physical = 9973 ; free virtual = 22137

Phase 4.3 Placer Reporting

Phase 4.3 Placer Reporting | Checksum: 1d1cffe7a

Time (s): cpu = 00:00:02 ; elapsed = 00:00:00.69 . Memory (MB): peak = 2352.984 ; gain = 74.023 ; free physical = 9973 ; free virtual = 22137

Phase 4.4 Final Placement Cleanup

Phase 4.4 Final Placement Cleanup | Checksum: 1d1cffe7a

Time (s): cpu = 00:00:02 ; elapsed = 00:00:00.69 . Memory (MB): peak = 2352.984 ; gain = 74.023 ; free physical = 9973 ; free virtual = 22137

Phase 4 Post Placement Optimization and Clean-Up | Checksum: 1d1cffe7a

Time (s): cpu = 00:00:02 ; elapsed = 00:00:00.69 . Memory (MB): peak = 2352.984 ; gain = 74.023 ; free physical = 9973 ; free virtual = 22137

Ending Placer Task | Checksum: 19b32f39b

Time (s): cpu = 00:00:02 ; elapsed = 00:00:00.69 . Memory (MB): peak = 2352.984 ; gain = 74.023 ; free physical = 9990 ; free virtual = 22154

INFO: [Common 17-83] Releasing license: Implementation

41 Infos, 1 Warnings, 0 Critical Warnings and 0 Errors encountered.

place\_design completed successfully

INFO: [Timing 38-480] Writing timing data to binary archive.

Writing placer database...

Writing XDEF routing.

Writing XDEF routing logical nets.

Writing XDEF routing special nets.

Write XDEF Complete: Time (s): cpu = 00:00:00.04 ; elapsed = 00:00:00.10 . Memory (MB): peak = 2352.984 ; gain = 0.000 ; free physical = 9990 ; free virtual = 22154

INFO: [Common 17-1381] The checkpoint '/nfs/home/n/n\_louvet/Coen316/lab3/vivado/lab3\_316/lab3\_316.runs/impl\_1/next\_address\_placed.dcp' has been generated.

INFO: [runtcl-4] Executing : report\_io -file next\_address\_io\_placed.rpt

report\_io: Time (s): cpu = 00:00:00.07 ; elapsed = 00:00:00.12 . Memory (MB): peak = 2352.984 ; gain = 0.000 ; free physical = 9985 ; free virtual = 22149

INFO: [runtcl-4] Executing : report\_utilization -file next\_address\_utilization\_placed.rpt -pb next\_address\_utilization\_placed.pb

report\_utilization: Time (s): cpu = 00:00:00.03 ; elapsed = 00:00:00.06 . Memory (MB): peak = 2352.984 ; gain = 0.000 ; free physical = 9993 ; free virtual = 22156

INFO: [runtcl-4] Executing : report\_control\_sets -verbose -file next\_address\_control\_sets\_placed.rpt

report\_control\_sets: Time (s): cpu = 00:00:00.02 ; elapsed = 00:00:00.04 . Memory (MB): peak = 2352.984 ; gain = 0.000 ; free physical = 9992 ; free virtual = 22156

Command: route\_design

Attempting to get a license for feature 'Implementation' and/or device 'xc7a100t'

INFO: [Common 17-349] Got license for feature 'Implementation' and/or device 'xc7a100t'

Running DRC as a precondition to command route\_design

INFO: [DRC 23-27] Running DRC with 8 threads

INFO: [Vivado\_Tcl 4-198] DRC finished with 0 Errors

INFO: [Vivado\_Tcl 4-199] Please refer to the DRC report (report\_drc) for more information.

Starting Routing Task

INFO: [Route 35-254] Multithreading enabled for route\_design using a maximum of 8 CPUs

Checksum: PlaceDB: e0240ba7 ConstDB: 0 ShapeSum: bb0ee7f4 RouteDB: 0

Phase 1 Build RT Design

Phase 1 Build RT Design | Checksum: 15ff9bcfc

Time (s): cpu = 00:00:16 ; elapsed = 00:00:13 . Memory (MB): peak = 2392.980 ; gain = 39.996 ; free physical = 9835 ; free virtual = 21999

Post Restoration Checksum: NetGraph: c83f053f NumContArr: 97bab7bd Constraints: 0 Timing: 0

Phase 2 Router Initialization

INFO: [Route 35-64] No timing constraints were detected. The router will operate in resource-optimization mode.

Phase 2.1 Fix Topology Constraints

Phase 2.1 Fix Topology Constraints | Checksum: 15ff9bcfc

Time (s): cpu = 00:00:16 ; elapsed = 00:00:13 . Memory (MB): peak = 2399.969 ; gain = 46.984 ; free physical = 9804 ; free virtual = 21967

Phase 2.2 Pre Route Cleanup

Phase 2.2 Pre Route Cleanup | Checksum: 15ff9bcfc

Time (s): cpu = 00:00:16 ; elapsed = 00:00:13 . Memory (MB): peak = 2399.969 ; gain = 46.984 ; free physical = 9804 ; free virtual = 21967

Number of Nodes with overlaps = 0

Phase 2 Router Initialization | Checksum: 111cc0823

Time (s): cpu = 00:00:16 ; elapsed = 00:00:13 . Memory (MB): peak = 2407.234 ; gain = 54.250 ; free physical = 9801 ; free virtual = 21965

Phase 3 Initial Routing

Phase 3 Initial Routing | Checksum: 180f0b0eb

Time (s): cpu = 00:00:16 ; elapsed = 00:00:13 . Memory (MB): peak = 2407.234 ; gain = 54.250 ; free physical = 9799 ; free virtual = 21963

Phase 4 Rip-up And Reroute

Phase 4.1 Global Iteration 0

Number of Nodes with overlaps = 2

Number of Nodes with overlaps = 0

Phase 4.1 Global Iteration 0 | Checksum: 6b463def

Time (s): cpu = 00:00:16 ; elapsed = 00:00:13 . Memory (MB): peak = 2407.234 ; gain = 54.250 ; free physical = 9799 ; free virtual = 21963

Phase 4 Rip-up And Reroute | Checksum: 6b463def

Time (s): cpu = 00:00:16 ; elapsed = 00:00:13 . Memory (MB): peak = 2407.234 ; gain = 54.250 ; free physical = 9799 ; free virtual = 21963

Phase 5 Delay and Skew Optimization

Phase 5 Delay and Skew Optimization | Checksum: 6b463def

Time (s): cpu = 00:00:16 ; elapsed = 00:00:13 . Memory (MB): peak = 2407.234 ; gain = 54.250 ; free physical = 9799 ; free virtual = 21963

Phase 6 Post Hold Fix

Phase 6.1 Hold Fix Iter

Phase 6.1 Hold Fix Iter | Checksum: 6b463def

Time (s): cpu = 00:00:16 ; elapsed = 00:00:13 . Memory (MB): peak = 2407.234 ; gain = 54.250 ; free physical = 9799 ; free virtual = 21963

Phase 6 Post Hold Fix | Checksum: 6b463def

Time (s): cpu = 00:00:16 ; elapsed = 00:00:13 . Memory (MB): peak = 2407.234 ; gain = 54.250 ; free physical = 9799 ; free virtual = 21963

Phase 7 Route finalize

Router Utilization Summary

Global Vertical Routing Utilization = 0.0145798 %

Global Horizontal Routing Utilization = 0.0135692 %

Routable Net Status\*

\*Does not include unroutable nets such as driverless and loadless.

Run report\_route\_status for detailed report.

Number of Failed Nets = 0

Number of Unrouted Nets = 0

Number of Partially Routed Nets = 0

Number of Node Overlaps = 0

Congestion Report

North Dir 1x1 Area, Max Cong = 16.2162%, No Congested Regions.

South Dir 1x1 Area, Max Cong = 16.2162%, No Congested Regions.

East Dir 1x1 Area, Max Cong = 5.88235%, No Congested Regions.

West Dir 1x1 Area, Max Cong = 5.88235%, No Congested Regions.

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Reporting congestion hotspots

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Direction: North

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Congested clusters found at Level 0

Effective congestion level: 0 Aspect Ratio: 1 Sparse Ratio: 0

Direction: South

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Congested clusters found at Level 0

Effective congestion level: 0 Aspect Ratio: 1 Sparse Ratio: 0

Direction: East

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Congested clusters found at Level 0

Effective congestion level: 0 Aspect Ratio: 1 Sparse Ratio: 0

Direction: West

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Congested clusters found at Level 0

Effective congestion level: 0 Aspect Ratio: 1 Sparse Ratio: 0

Phase 7 Route finalize | Checksum: 6b463def

Time (s): cpu = 00:00:16 ; elapsed = 00:00:13 . Memory (MB): peak = 2408.234 ; gain = 55.250 ; free physical = 9799 ; free virtual = 21963

Phase 8 Verifying routed nets

Verification completed successfully

Phase 8 Verifying routed nets | Checksum: 6b463def

Time (s): cpu = 00:00:17 ; elapsed = 00:00:13 . Memory (MB): peak = 2411.234 ; gain = 58.250 ; free physical = 9798 ; free virtual = 21962

Phase 9 Depositing Routes

Phase 9 Depositing Routes | Checksum: 499e74b3

Time (s): cpu = 00:00:17 ; elapsed = 00:00:13 . Memory (MB): peak = 2411.234 ; gain = 58.250 ; free physical = 9798 ; free virtual = 21962

INFO: [Route 35-16] Router Completed Successfully

Time (s): cpu = 00:00:17 ; elapsed = 00:00:13 . Memory (MB): peak = 2411.234 ; gain = 58.250 ; free physical = 9833 ; free virtual = 21997

Routing Is Done.

INFO: [Common 17-83] Releasing license: Implementation

54 Infos, 1 Warnings, 0 Critical Warnings and 0 Errors encountered.

route\_design completed successfully

route\_design: Time (s): cpu = 00:00:18 ; elapsed = 00:00:16 . Memory (MB): peak = 2411.238 ; gain = 58.254 ; free physical = 9833 ; free virtual = 21997

INFO: [Timing 38-480] Writing timing data to binary archive.

Writing placer database...

Writing XDEF routing.

Writing XDEF routing logical nets.

Writing XDEF routing special nets.

Write XDEF Complete: Time (s): cpu = 00:00:00.09 ; elapsed = 00:00:00.12 . Memory (MB): peak = 2411.238 ; gain = 0.000 ; free physical = 9831 ; free virtual = 21996

INFO: [Common 17-1381] The checkpoint '/nfs/home/n/n\_louvet/Coen316/lab3/vivado/lab3\_316/lab3\_316.runs/impl\_1/next\_address\_routed.dcp' has been generated.

INFO: [runtcl-4] Executing : report\_drc -file next\_address\_drc\_routed.rpt -pb next\_address\_drc\_routed.pb -rpx next\_address\_drc\_routed.rpx

Command: report\_drc -file next\_address\_drc\_routed.rpt -pb next\_address\_drc\_routed.pb -rpx next\_address\_drc\_routed.rpx

INFO: [DRC 23-27] Running DRC with 8 threads

INFO: [Coretcl 2-168] The results of DRC are in file /nfs/home/n/n\_louvet/Coen316/lab3/vivado/lab3\_316/lab3\_316.runs/impl\_1/next\_address\_drc\_routed.rpt.

report\_drc completed successfully

INFO: [runtcl-4] Executing : report\_methodology -file next\_address\_methodology\_drc\_routed.rpt -pb next\_address\_methodology\_drc\_routed.pb -rpx next\_address\_methodology\_drc\_routed.rpx

Command: report\_methodology -file next\_address\_methodology\_drc\_routed.rpt -pb next\_address\_methodology\_drc\_routed.pb -rpx next\_address\_methodology\_drc\_routed.rpx

INFO: [Timing 38-35] Done setting XDC timing constraints.

INFO: [Timing 38-35] Done setting XDC timing constraints.

INFO: [DRC 23-133] Running Methodology with 8 threads

INFO: [Coretcl 2-1520] The results of Report Methodology are in file /nfs/home/n/n\_louvet/Coen316/lab3/vivado/lab3\_316/lab3\_316.runs/impl\_1/next\_address\_methodology\_drc\_routed.rpt.

report\_methodology completed successfully

INFO: [runtcl-4] Executing : report\_power -file next\_address\_power\_routed.rpt -pb next\_address\_power\_summary\_routed.pb -rpx next\_address\_power\_routed.rpx

Command: report\_power -file next\_address\_power\_routed.rpt -pb next\_address\_power\_summary\_routed.pb -rpx next\_address\_power\_routed.rpx

WARNING: [Power 33-232] No user defined clocks were found in the design!

Resolution: Please specify clocks using create\_clock/create\_generated\_clock for sequential elements. For pure combinatorial circuits, please specify a virtual clock, otherwise the vectorless estimation might be inaccurate

INFO: [Timing 38-35] Done setting XDC timing constraints.

Running Vector-less Activity Propagation...

Finished Running Vector-less Activity Propagation

66 Infos, 2 Warnings, 0 Critical Warnings and 0 Errors encountered.

report\_power completed successfully

INFO: [runtcl-4] Executing : report\_route\_status -file next\_address\_route\_status.rpt -pb next\_address\_route\_status.pb

INFO: [runtcl-4] Executing : report\_timing\_summary -max\_paths 10 -file next\_address\_timing\_summary\_routed.rpt -pb next\_address\_timing\_summary\_routed.pb -rpx next\_address\_timing\_summary\_routed.rpx -warn\_on\_violation

INFO: [Timing 38-91] UpdateTimingParams: Speed grade: -1, Delay Type: min\_max, Timing Stage: Requireds.

INFO: [Timing 38-191] Multithreading enabled for timing update using a maximum of 8 CPUs

WARNING: [Timing 38-313] There are no user specified timing constraints. Timing constraints are needed for proper timing analysis.

INFO: [runtcl-4] Executing : report\_incremental\_reuse -file next\_address\_incremental\_reuse\_routed.rpt

INFO: [Vivado\_Tcl 4-545] No incremental reuse to report, no incremental placement and routing data was found.

INFO: [runtcl-4] Executing : report\_clock\_utilization -file next\_address\_clock\_utilization\_routed.rpt

INFO: [runtcl-4] Executing : report\_bus\_skew -warn\_on\_violation -file next\_address\_bus\_skew\_routed.rpt -pb next\_address\_bus\_skew\_routed.pb -rpx next\_address\_bus\_skew\_routed.rpx

INFO: [Timing 38-91] UpdateTimingParams: Speed grade: -1, Delay Type: min\_max, Timing Stage: Requireds.

INFO: [Timing 38-191] Multithreading enabled for timing update using a maximum of 8 CPUs

INFO: [Common 17-206] Exiting Vivado at Mon Nov 6 18:00:59 2023...

\*\*\* Running vivado

with args -log next\_address.vdi -applog -m64 -product Vivado -messageDb vivado.pb -mode batch -source next\_address.tcl -notrace

\*\*\*\*\*\* Vivado v2018.2 (64-bit)

\*\*\*\* SW Build 2258646 on Thu Jun 14 20:02:38 MDT 2018

\*\*\*\* IP Build 2256618 on Thu Jun 14 22:10:49 MDT 2018

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source next\_address.tcl -notrace

Command: open\_checkpoint next\_address\_routed.dcp

Starting open\_checkpoint Task

Time (s): cpu = 00:00:00.04 ; elapsed = 00:00:00.13 . Memory (MB): peak = 1277.117 ; gain = 0.000 ; free physical = 10745 ; free virtual = 22910

INFO: [Netlist 29-17] Analyzing 14 Unisim elements for replacement

INFO: [Netlist 29-28] Unisim Transformation completed in 0 CPU seconds

INFO: [Project 1-479] Netlist was created with Vivado 2018.2

INFO: [Device 21-403] Loading part xc7a100tcsg324-1

INFO: [Project 1-570] Preparing netlist for logic optimization

INFO: [Timing 38-478] Restoring timing data from binary archive.

INFO: [Timing 38-479] Binary timing data restore complete.

INFO: [Project 1-856] Restoring constraints from binary archive.

INFO: [Project 1-853] Binary constraint restore complete.

Reading XDEF placement.

Reading placer database...

Reading XDEF routing.

Read XDEF File: Time (s): cpu = 00:00:00.07 ; elapsed = 00:00:00.22 . Memory (MB): peak = 2079.066 ; gain = 0.004 ; free physical = 10012 ; free virtual = 22177

Restored from archive | CPU: 0.220000 secs | Memory: 0.960587 MB |

Finished XDEF File Restore: Time (s): cpu = 00:00:00.07 ; elapsed = 00:00:00.22 . Memory (MB): peak = 2079.066 ; gain = 0.004 ; free physical = 10012 ; free virtual = 22177

INFO: [Project 1-111] Unisim Transformation Summary:

No Unisim elements were transformed.

INFO: [Project 1-604] Checkpoint was created with Vivado v2018.2 (64-bit) build 2258646

open\_checkpoint: Time (s): cpu = 00:00:17 ; elapsed = 00:01:09 . Memory (MB): peak = 2079.066 ; gain = 801.953 ; free physical = 10012 ; free virtual = 22176

Command: write\_bitstream -force next\_address.bit

Attempting to get a license for feature 'Implementation' and/or device 'xc7a100t'

INFO: [Common 17-349] Got license for feature 'Implementation' and/or device 'xc7a100t'

Running DRC as a precondition to command write\_bitstream

INFO: [IP\_Flow 19-234] Refreshing IP repositories

INFO: [IP\_Flow 19-1704] No user IP repositories specified

INFO: [IP\_Flow 19-2313] Loaded Vivado IP repository '/CMC/tools/xilinx/Vivado\_2018.2/Vivado/2018.2/data/ip'.

INFO: [DRC 23-27] Running DRC with 8 threads

WARNING: [DRC CFGBVS-1] Missing CFGBVS and CONFIG\_VOLTAGE Design Properties: Neither the CFGBVS nor CONFIG\_VOLTAGE voltage property is set in the current\_design. Configuration bank voltage select (CFGBVS) must be set to VCCO or GND, and CONFIG\_VOLTAGE must be set to the correct configuration voltage, in order to determine the I/O voltage support for the pins in bank 0. It is suggested to specify these either using the 'Edit Device Properties' function in the GUI or directly in the XDC file using the following syntax:

set\_property CFGBVS value1 [current\_design]

#where value1 is either VCCO or GND

set\_property CONFIG\_VOLTAGE value2 [current\_design]

#where value2 is the voltage provided to configuration bank 0

Refer to the device configuration user guide for more information.

WARNING: [DRC PDRC-153] Gated clock check: Net next\_pc\_reg[2]\_i\_2\_n\_0 is a gated clock net sourced by a combinational pin next\_pc\_reg[2]\_i\_2/O, cell next\_pc\_reg[2]\_i\_2. This is not good design practice and will likely impact performance. For SLICE registers, for example, use the CE pin to control the loading of data.

INFO: [Vivado 12-3199] DRC finished with 0 Errors, 2 Warnings

INFO: [Vivado 12-3200] Please refer to the DRC report (report\_drc) for more information.

INFO: [Designutils 20-2272] Running write\_bitstream with 8 threads.

Loading data files...

Loading site data...

Loading route data...

Processing options...

Creating bitmap...

Creating bitstream...

Writing bitstream ./next\_address.bit...

INFO: [Vivado 12-1842] Bitgen Completed Successfully.

INFO: [Common 17-83] Releasing license: Implementation

21 Infos, 2 Warnings, 0 Critical Warnings and 0 Errors encountered.

write\_bitstream completed successfully

write\_bitstream: Time (s): cpu = 00:00:08 ; elapsed = 00:00:12 . Memory (MB): peak = 2550.906 ; gain = 471.840 ; free physical = 9941 ; free virtual = 22114

INFO: [Common 17-206] Exiting Vivado at Mon Nov 6 18:02:38 2023...

**Vivado Implementation**

\*\*\* Running vivado

with args -log next\_address.vds -m64 -product Vivado -mode batch -messageDb vivado.pb -notrace -source next\_address.tcl

\*\*\*\*\*\* Vivado v2018.2 (64-bit)

\*\*\*\* SW Build 2258646 on Thu Jun 14 20:02:38 MDT 2018

\*\*\*\* IP Build 2256618 on Thu Jun 14 22:10:49 MDT 2018

\*\* Copyright 1986-2018 Xilinx, Inc. All Rights Reserved.

source next\_address.tcl -notrace

Command: synth\_design -top next\_address -part xc7a100tcsg324-1

Starting synth\_design

Attempting to get a license for feature 'Synthesis' and/or device 'xc7a100t'

INFO: [Common 17-349] Got license for feature 'Synthesis' and/or device 'xc7a100t'

INFO: Launching helper process for spawning children vivado processes

INFO: Helper process launched with PID 25218

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Starting RTL Elaboration : Time (s): cpu = 00:00:01 ; elapsed = 00:00:03 . Memory (MB): peak = 1401.578 ; gain = 85.805 ; free physical = 10685 ; free virtual = 22787

---------------------------------------------------------------------------------

INFO: [Synth 8-638] synthesizing module 'next\_address' [/nfs/home/n/n\_louvet/Coen316/lab3/vivado/lab3\_316/lab3\_316.srcs/sources\_1/imports/lab3/nextaddress\_board.vhd:15]

WARNING: [Synth 8-614] signal 'branch\_offset' is read in the process but is not in the sensitivity list [/nfs/home/n/n\_louvet/Coen316/lab3/vivado/lab3\_316/lab3\_316.srcs/sources\_1/imports/lab3/nextaddress\_board.vhd:64]

INFO: [Synth 8-256] done synthesizing module 'next\_address' (1#1) [/nfs/home/n/n\_louvet/Coen316/lab3/vivado/lab3\_316/lab3\_316.srcs/sources\_1/imports/lab3/nextaddress\_board.vhd:15]

---------------------------------------------------------------------------------

Finished RTL Elaboration : Time (s): cpu = 00:00:02 ; elapsed = 00:00:04 . Memory (MB): peak = 1446.219 ; gain = 130.445 ; free physical = 10690 ; free virtual = 22795

---------------------------------------------------------------------------------

Report Check Netlist:

+------+------------------+-------+---------+-------+------------------+

| |Item |Errors |Warnings |Status |Description |

+------+------------------+-------+---------+-------+------------------+

|1 |multi\_driven\_nets | 0| 0|Passed |Multi driven nets |

+------+------------------+-------+---------+-------+------------------+

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Start Handling Custom Attributes

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Finished Handling Custom Attributes : Time (s): cpu = 00:00:02 ; elapsed = 00:00:04 . Memory (MB): peak = 1446.219 ; gain = 130.445 ; free physical = 10689 ; free virtual = 22794

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Finished RTL Optimization Phase 1 : Time (s): cpu = 00:00:02 ; elapsed = 00:00:04 . Memory (MB): peak = 1446.219 ; gain = 130.445 ; free physical = 10689 ; free virtual = 22794

---------------------------------------------------------------------------------

INFO: [Device 21-403] Loading part xc7a100tcsg324-1

INFO: [Project 1-570] Preparing netlist for logic optimization

Processing XDC Constraints

Initializing timing engine

Parsing XDC File [/nfs/home/n/n\_louvet/Coen316/lab3/vivado/lab3\_316/lab3\_316.srcs/constrs\_1/imports/DO/next\_address.xdc]

Finished Parsing XDC File [/nfs/home/n/n\_louvet/Coen316/lab3/vivado/lab3\_316/lab3\_316.srcs/constrs\_1/imports/DO/next\_address.xdc]

INFO: [Project 1-236] Implementation specific constraints were found while reading constraint file [/nfs/home/n/n\_louvet/Coen316/lab3/vivado/lab3\_316/lab3\_316.srcs/constrs\_1/imports/DO/next\_address.xdc]. These constraints will be ignored for synthesis but will be used in implementation. Impacted constraints are listed in the file [.Xil/next\_address\_propImpl.xdc].

Resolution: To avoid this warning, move constraints listed in [.Xil/next\_address\_propImpl.xdc] to another XDC file and exclude this new file from synthesis with the used\_in\_synthesis property (File Properties dialog in GUI) and re-run elaboration/synthesis.

Completed Processing XDC Constraints

INFO: [Project 1-111] Unisim Transformation Summary:

No Unisim elements were transformed.

Constraint Validation Runtime : Time (s): cpu = 00:00:00 ; elapsed = 00:00:00.01 . Memory (MB): peak = 1797.965 ; gain = 0.000 ; free physical = 10358 ; free virtual = 22494

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Finished Constraint Validation : Time (s): cpu = 00:00:10 ; elapsed = 00:00:40 . Memory (MB): peak = 1797.965 ; gain = 482.191 ; free physical = 10464 ; free virtual = 22600

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Start Loading Part and Timing Information

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Loading part: xc7a100tcsg324-1

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Finished Loading Part and Timing Information : Time (s): cpu = 00:00:10 ; elapsed = 00:00:40 . Memory (MB): peak = 1797.965 ; gain = 482.191 ; free physical = 10464 ; free virtual = 22600

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Start Applying 'set\_property' XDC Constraints

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Finished applying 'set\_property' XDC Constraints : Time (s): cpu = 00:00:10 ; elapsed = 00:00:40 . Memory (MB): peak = 1797.965 ; gain = 482.191 ; free physical = 10465 ; free virtual = 22601

---------------------------------------------------------------------------------

WARNING: [Synth 8-327] inferring latch for variable 'next\_pc\_reg' [/nfs/home/n/n\_louvet/Coen316/lab3/vivado/lab3\_316/lab3\_316.srcs/sources\_1/imports/lab3/nextaddress\_board.vhd:36]

---------------------------------------------------------------------------------

Finished RTL Optimization Phase 2 : Time (s): cpu = 00:00:10 ; elapsed = 00:00:40 . Memory (MB): peak = 1797.965 ; gain = 482.191 ; free physical = 10457 ; free virtual = 22593

---------------------------------------------------------------------------------

Report RTL Partitions:

+-+--------------+------------+----------+

| |RTL Partition |Replication |Instances |

+-+--------------+------------+----------+

+-+--------------+------------+----------+

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Start RTL Component Statistics

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Detailed RTL Component Info :

+---Adders :

2 Input 32 Bit Adders := 1

2 Input 4 Bit Adders := 1

+---Muxes :

2 Input 32 Bit Muxes := 2

4 Input 32 Bit Muxes := 2

4 Input 1 Bit Muxes := 1

---------------------------------------------------------------------------------

Finished RTL Component Statistics

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---------------------------------------------------------------------------------

Start RTL Hierarchical Component Statistics

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Hierarchical RTL Component report

Module next\_address

Detailed RTL Component Info :

+---Adders :

2 Input 32 Bit Adders := 1

2 Input 4 Bit Adders := 1

+---Muxes :

2 Input 32 Bit Muxes := 2

4 Input 32 Bit Muxes := 2

4 Input 1 Bit Muxes := 1

---------------------------------------------------------------------------------

Finished RTL Hierarchical Component Statistics

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---------------------------------------------------------------------------------

Start Part Resource Summary

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Part Resources:

DSPs: 240 (col length:80)

BRAMs: 270 (col length: RAMB18 80 RAMB36 40)

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Finished Part Resource Summary

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Start Cross Boundary and Area Optimization

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Warning: Parallel synthesis criteria is not met

WARNING: [Synth 8-3332] Sequential element (next\_pc\_reg[31]) is unused and will be removed from module next\_address.

WARNING: [Synth 8-3332] Sequential element (next\_pc\_reg[30]) is unused and will be removed from module next\_address.

WARNING: [Synth 8-3332] Sequential element (next\_pc\_reg[29]) is unused and will be removed from module next\_address.

WARNING: [Synth 8-3332] Sequential element (next\_pc\_reg[28]) is unused and will be removed from module next\_address.

WARNING: [Synth 8-3332] Sequential element (next\_pc\_reg[27]) is unused and will be removed from module next\_address.

WARNING: [Synth 8-3332] Sequential element (next\_pc\_reg[26]) is unused and will be removed from module next\_address.

WARNING: [Synth 8-3332] Sequential element (next\_pc\_reg[25]) is unused and will be removed from module next\_address.

WARNING: [Synth 8-3332] Sequential element (next\_pc\_reg[24]) is unused and will be removed from module next\_address.

WARNING: [Synth 8-3332] Sequential element (next\_pc\_reg[23]) is unused and will be removed from module next\_address.

WARNING: [Synth 8-3332] Sequential element (next\_pc\_reg[22]) is unused and will be removed from module next\_address.

WARNING: [Synth 8-3332] Sequential element (next\_pc\_reg[21]) is unused and will be removed from module next\_address.

WARNING: [Synth 8-3332] Sequential element (next\_pc\_reg[20]) is unused and will be removed from module next\_address.

WARNING: [Synth 8-3332] Sequential element (next\_pc\_reg[19]) is unused and will be removed from module next\_address.

WARNING: [Synth 8-3332] Sequential element (next\_pc\_reg[18]) is unused and will be removed from module next\_address.

WARNING: [Synth 8-3332] Sequential element (next\_pc\_reg[17]) is unused and will be removed from module next\_address.

WARNING: [Synth 8-3332] Sequential element (next\_pc\_reg[16]) is unused and will be removed from module next\_address.

WARNING: [Synth 8-3332] Sequential element (next\_pc\_reg[15]) is unused and will be removed from module next\_address.

WARNING: [Synth 8-3332] Sequential element (next\_pc\_reg[14]) is unused and will be removed from module next\_address.

WARNING: [Synth 8-3332] Sequential element (next\_pc\_reg[13]) is unused and will be removed from module next\_address.

WARNING: [Synth 8-3332] Sequential element (next\_pc\_reg[12]) is unused and will be removed from module next\_address.

WARNING: [Synth 8-3332] Sequential element (next\_pc\_reg[11]) is unused and will be removed from module next\_address.

WARNING: [Synth 8-3332] Sequential element (next\_pc\_reg[10]) is unused and will be removed from module next\_address.

WARNING: [Synth 8-3332] Sequential element (next\_pc\_reg[9]) is unused and will be removed from module next\_address.

WARNING: [Synth 8-3332] Sequential element (next\_pc\_reg[8]) is unused and will be removed from module next\_address.

WARNING: [Synth 8-3332] Sequential element (next\_pc\_reg[7]) is unused and will be removed from module next\_address.

WARNING: [Synth 8-3332] Sequential element (next\_pc\_reg[6]) is unused and will be removed from module next\_address.

WARNING: [Synth 8-3332] Sequential element (next\_pc\_reg[5]) is unused and will be removed from module next\_address.

WARNING: [Synth 8-3332] Sequential element (next\_pc\_reg[4]) is unused and will be removed from module next\_address.

WARNING: [Synth 8-3332] Sequential element (next\_pc\_reg[3]) is unused and will be removed from module next\_address.

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Finished Cross Boundary and Area Optimization : Time (s): cpu = 00:00:11 ; elapsed = 00:00:41 . Memory (MB): peak = 1797.965 ; gain = 482.191 ; free physical = 10446 ; free virtual = 22584

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Report RTL Partitions:

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| |RTL Partition |Replication |Instances |

+-+--------------+------------+----------+

+-+--------------+------------+----------+

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Start Applying XDC Timing Constraints

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Finished Applying XDC Timing Constraints : Time (s): cpu = 00:00:15 ; elapsed = 00:00:52 . Memory (MB): peak = 1797.965 ; gain = 482.191 ; free physical = 10321 ; free virtual = 22466

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Start Timing Optimization

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Finished Timing Optimization : Time (s): cpu = 00:00:15 ; elapsed = 00:00:52 . Memory (MB): peak = 1797.965 ; gain = 482.191 ; free physical = 10321 ; free virtual = 22466

---------------------------------------------------------------------------------

Report RTL Partitions:

+-+--------------+------------+----------+

| |RTL Partition |Replication |Instances |

+-+--------------+------------+----------+

+-+--------------+------------+----------+

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Start Technology Mapping

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Finished Technology Mapping : Time (s): cpu = 00:00:15 ; elapsed = 00:00:52 . Memory (MB): peak = 1797.965 ; gain = 482.191 ; free physical = 10321 ; free virtual = 22466

---------------------------------------------------------------------------------

Report RTL Partitions:

+-+--------------+------------+----------+

| |RTL Partition |Replication |Instances |

+-+--------------+------------+----------+

+-+--------------+------------+----------+

---------------------------------------------------------------------------------

Start IO Insertion

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Start Flattening Before IO Insertion

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Finished Flattening Before IO Insertion

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---------------------------------------------------------------------------------

Start Final Netlist Cleanup

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Finished Final Netlist Cleanup

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Finished IO Insertion : Time (s): cpu = 00:00:16 ; elapsed = 00:00:52 . Memory (MB): peak = 1797.965 ; gain = 482.191 ; free physical = 10321 ; free virtual = 22465

---------------------------------------------------------------------------------

Report Check Netlist:

+------+------------------+-------+---------+-------+------------------+

| |Item |Errors |Warnings |Status |Description |

+------+------------------+-------+---------+-------+------------------+

|1 |multi\_driven\_nets | 0| 0|Passed |Multi driven nets |

+------+------------------+-------+---------+-------+------------------+

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Start Renaming Generated Instances

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Finished Renaming Generated Instances : Time (s): cpu = 00:00:16 ; elapsed = 00:00:52 . Memory (MB): peak = 1797.965 ; gain = 482.191 ; free physical = 10321 ; free virtual = 22465

---------------------------------------------------------------------------------

Report RTL Partitions:

+-+--------------+------------+----------+

| |RTL Partition |Replication |Instances |

+-+--------------+------------+----------+

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Start Rebuilding User Hierarchy

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Finished Rebuilding User Hierarchy : Time (s): cpu = 00:00:16 ; elapsed = 00:00:52 . Memory (MB): peak = 1797.965 ; gain = 482.191 ; free physical = 10321 ; free virtual = 22465

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Start Renaming Generated Ports

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Finished Renaming Generated Ports : Time (s): cpu = 00:00:16 ; elapsed = 00:00:52 . Memory (MB): peak = 1797.965 ; gain = 482.191 ; free physical = 10321 ; free virtual = 22465

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Start Handling Custom Attributes

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Finished Handling Custom Attributes : Time (s): cpu = 00:00:16 ; elapsed = 00:00:52 . Memory (MB): peak = 1797.965 ; gain = 482.191 ; free physical = 10321 ; free virtual = 22465

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Start Renaming Generated Nets

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Finished Renaming Generated Nets : Time (s): cpu = 00:00:16 ; elapsed = 00:00:52 . Memory (MB): peak = 1797.965 ; gain = 482.191 ; free physical = 10321 ; free virtual = 22465

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Start Writing Synthesis Report

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Report BlackBoxes:

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| |BlackBox name |Instances |

+-+--------------+----------+

+-+--------------+----------+

Report Cell Usage:

+------+-----+------+

| |Cell |Count |

+------+-----+------+

|1 |LUT2 | 3|

|2 |LUT3 | 2|

|3 |LUT4 | 2|

|4 |LUT5 | 2|

|5 |LUT6 | 3|

|6 |LD | 3|

|7 |IBUF | 14|

|8 |OBUF | 3|

+------+-----+------+

Report Instance Areas:

+------+---------+-------+------+

| |Instance |Module |Cells |

+------+---------+-------+------+

|1 |top | | 32|

+------+---------+-------+------+

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Finished Writing Synthesis Report : Time (s): cpu = 00:00:16 ; elapsed = 00:00:52 . Memory (MB): peak = 1797.965 ; gain = 482.191 ; free physical = 10321 ; free virtual = 22465

---------------------------------------------------------------------------------

Synthesis finished with 0 errors, 0 critical warnings and 30 warnings.

Synthesis Optimization Runtime : Time (s): cpu = 00:00:09 ; elapsed = 00:00:19 . Memory (MB): peak = 1797.965 ; gain = 130.445 ; free physical = 10375 ; free virtual = 22520

Synthesis Optimization Complete : Time (s): cpu = 00:00:16 ; elapsed = 00:00:52 . Memory (MB): peak = 1797.965 ; gain = 482.191 ; free physical = 10386 ; free virtual = 22531

INFO: [Project 1-571] Translating synthesized netlist

INFO: [Netlist 29-17] Analyzing 17 Unisim elements for replacement

INFO: [Netlist 29-28] Unisim Transformation completed in 0 CPU seconds

INFO: [Project 1-570] Preparing netlist for logic optimization

INFO: [Opt 31-138] Pushed 0 inverter(s) to 0 load pin(s).

INFO: [Project 1-111] Unisim Transformation Summary:

A total of 3 instances were transformed.

LD => LDCE: 3 instances

INFO: [Common 17-83] Releasing license: Synthesis

14 Infos, 31 Warnings, 0 Critical Warnings and 0 Errors encountered.

synth\_design completed successfully

synth\_design: Time (s): cpu = 00:00:17 ; elapsed = 00:00:53 . Memory (MB): peak = 1821.969 ; gain = 518.844 ; free physical = 10375 ; free virtual = 22520

WARNING: [Constraints 18-5210] No constraint will be written out.

INFO: [Common 17-1381] The checkpoint '/nfs/home/n/n\_louvet/Coen316/lab3/vivado/lab3\_316/lab3\_316.runs/synth\_1/next\_address.dcp' has been generated.

INFO: [runtcl-4] Executing : report\_utilization -file next\_address\_utilization\_synth.rpt -pb next\_address\_utilization\_synth.pb

report\_utilization: Time (s): cpu = 00:00:00.07 ; elapsed = 00:00:00.11 . Memory (MB): peak = 1845.988 ; gain = 0.000 ; free physical = 10374 ; free virtual = 22519

INFO: [Common 17-206] Exiting Vivado at Mon Nov 6 17:58:52 2023...